REMARKS

This paper is responsive to the Non-Final Office Action dated January 10, 2006. Claims 1-60 are pending. Claims 2-20, 22, 23 and 29-60 are withdrawn from consideration. Claims 1, 21 and 24-28 were examined, and all were rejected.

Amendments to the Specification

Several paragraphs have been amended to correct minor typographical errors. None adds new matter.

Claim Rejections - 35 U.S.C. § 112

Claims 1, 21 and 24-28 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicant respectfully traverses this rejection.

In claim 1, line 4 (and also in claim 25, line 2), the Examiner indicates that is not clear what is meant by the phrase "of like type". In the previous response filed July 21, 2005, Applicant noted that independent claims 1, 39 and 55, and dependent claim 25 were amended to recite a plurality of (or a group of one or more) series selection devices of like type at a recited end of a NAND string. Such additional limitation does not necessarily require that the selection devices at a particular end of the NAND string are the same type as the memory cells devices of the NAND string (although in certain other claims this is specifically claimed), nor does it require that the selection devices at one end of a given NAND string are necessarily the same type as the selection devices at the other end of the given NAND string, but merely that the devices of a given plurality of series selection devices are identical in type. For example, two devices having different threshold voltages (as manufactured) are *not* "of like type."

Regarding claim 25, the Examiner also expressed concern that the claim includes a recitation of a "second plurality of series selection devices" and there is no recited "first plurality of series selection devices." Applicant notes that claim 1 includes a recitation of "said NAND strings including at a *first end* thereof a *respective plurality of series selection devices* of like

type." Such recitation is believed to provide ample antecedent basis for the first plurality of series selection devices of each NAND string.

Applicant believes that these claim limitation are clear, but is certainly open to discussing a textual change if the Examiner feels that such would be desirable.

Claim Rejections - 35 U.S.C. § 102

Claims 1, 21, 24 and 27-28 stand rejected under 35 U.S.C.§ 102(b)/(e) as being anticipated by Sakui et al. (U.S. Patent No. 6,411,548) or Scheuerlein et al. (Patent Publication No. 2004/0125629). Applicant respectfully traverses this rejection.

Regarding claim 1, the Examiner advances the position that Sakui discloses, in his memory array, "NAND strings including at a first end thereof a respective plurality of series selection devices," citing the select gate transistor S2 shown in Fig. 47. Applicant respectfully submits that Sakui merely discloses a *single* series selection device (e.g., transistor S2) at a first end of each NAND string. Sakui does not disclose a *respective* plurality of series selection devices at a first end of each NAND string, as required by the claim language.

The Examiner also advances the position that Scheuerlein discloses, in his memory array, "NAND strings including at a first end thereof a respective plurality of series selection devices," citing Figs. 1-3. Applicant respectfully submits that Scheuerlein merely discloses a *single* series selection device (e.g., the transistor 147 having BSEL1 coupled to its gate, as shown in Fig. 3; alternatively, the transistor 148 at the other end of the NAND string having BSEL2 coupled to its gate) at a first end of each NAND string. Scheuerlein does not disclose a *respective* plurality of series selection devices at a first end of each NAND string, as required by the claim language. Nowhere does Scheuerlein disclose more than one block select signal at each end of a NAND string, each coupled to a single respective block select transistor at the same end of the NAND string.

Applicant respectfully submits that no prima facie case has been made out, as neither reference alone (or together) teaches or suggests all the limitations of the claim, and requests the Examiner to withdraw this rejection.

Claim Rejections - 35 U.S.C. § 103

Claims 25-26 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sakui in view of Chen et al. (U.S. Patent No. 6,266,275) or Ichige et al. (Patent Publication No. 2004/0152262). Applicant respectfully traverses this rejection in part.

Regarding claim 25, the Examiner states that Sakui discloses all claimed limitations of claim 21 from which claim 25 depends. As stated above, Applicant respectfully submits that Sakui does not disclose all the limitations of claim 1, and thus cannot be seen as disclosing all the limitations of claim 21. Nevertheless, as the Examiner has observed, Ichige in Fig. 50 discloses a NAND string having three series select devices at one end (the transistors gated by SSL1, SSL2, and SSL3 coupling each NAND string to a respective bit line such as BL0, BL1), and further having three series select devices at the other end (the transistors gated by GSL1, GSL2, and GSL3 coupling each NAND string to a common source line SOURCE).

Regarding claim 26, the Examiner states that Sakui also discloses a pair of NAND strings arranged so that a first group of control signals couples the respective second end of one string of the pair to a global array line associated with the pair. In support of this position, the Examiner cites GSLa and SSLb as the first group of control signals, and GSLb and SSLa as the second group of control signals, followed by an argument as to how *one* of the signals in a particular group of signals couples the various ends of particular NAND strings to particular nodes. The fallacy of this construction is that nowhere does Sakui disclose the *group* of signals coupling one end of a NAND string to a particular node. Claim 26 (by way of the limitations of claim 25) recites a plurality of series selection devices at each end of each NAND string, and recites, *inter alia*, one group of signals coupling one end of a given NAND string to a certain node, and another group of signals coupling the other end of the given NAND string to another node. Sakui only shows one series selection device at each end of his NAND strings, and likewise only shows one select signal at each end of each NAND string.

Applicant notes that the construction advanced by the Examiner requires each alleged group of control signals to include two such signals. For example, the first group of control signals includes GSLa and SSLb, and the second group of control signals includes GSLb and SSLa. But as stated above, if such a first group includes GSLa and SSLb, then *both* control

signals of the group must couple one end of a NAND string to its stated node to satisfy the claim language "arranged so that a first *group* of control signals couples the respective second *end* of *one string* of the pair to a global array line...". One cannot identify an alleged group of signals in the Sakui reference, then proceed to split these signals into individual ones when attempting to read the claim onto the reference.

Neither does the structure disclosed by Ichige rise to the limitations of claim 26. As shown in his Fig. 50, one group of control signals are connected respectively to three series select devices at one end of a NAND string (e.g., the transistors gated by SSL1, SSL2, and SSL3) and couple each NAND string to a respective bit line (e.g., BL0, BL1). Another group of control signals are connected respectively to three series select devices at the other end of each NAND string (e.g., the transistors gated by GSL1, GSL2, and GSL3) and couple each NAND string to a common source line (e.g., SOURCE). Nowhere does Ichige show the same control signals associated with series selection devices at one end (e.g., the bit line end) of certain NAND strings, yet *also* associated with series selection devices at the other end (e.g., the "source line" or bias node end) of certain other NAND strings.

Said differently, nowhere does Ichige show a first group of control signals which couples the respective second end of one string of a pair of NAND strings to a global array line associated with the pair, and which first group of control signals also couples the respective first end of the other string of the pair to a respective bias node, nor does Ichige show a second group of control signals which couples the respective first end of said one string of the pair to a respective bias node, and which second group of control signals couples the respective second end of the other string of the pair to the global array line associated with the pair, as required by the language of the claim.

Applicant respectfully submits that no *prima facie* case has been made out, as the references of record do not teach or suggest all the limitations of the claim. Consequently, Applicant respectfully requests the rejection be withdrawn as to claim 26.

Other Amendments

Notwithstanding the arguments presented above, Applicant has amended the claims in an attempt to secure a more timely allowance of the application. Claim 1 has been amended to incorporate the limitations of claim 26 (and thus the limitations of intervening claims 21 and 25). Claims 21, 25 and 26 have thus been canceled.

Claims 3 and 22 (currently withdrawn) and claim 27 previously depended from claim 21 and have been amended to now depend from amended claim 1. Claim 24 has also been canceled.

Summary

Claims 1-20, 22, 23 and 27-60 remain in the case (claims 2-20, 22, 23 and 29-60 being withdrawn from consideration). Claims 1, 27 and 28 remain under examination, and are believed to be allowable over the art of record. A Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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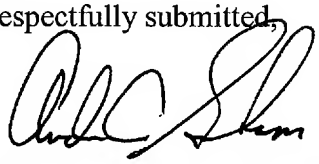
Respectfully submitted,



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